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InGaZnO Tunnel and Junction Transistors Based on Vertically Stacked Black Phosphorus/InGaZnO Heterojunctions

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The rapid development of mobile and internet-of-thing devices demands continuous scaling of metal–insulator–semiconductor field-effect transistors for high-resolution and low-power displays. However, such technology is limited by inadequate scaling of supply voltage and sophisticated dielectric engineering. Here, to enable continued scaling, indium–gallium–zinc-oxide (InGaZnO) tunnel field-effect transistor (TFET) and junction field-effect transistor (JFET) are designed and fabricated based on vertically stacked black phosphorus (BP)/InGaZnO van der Waals heterojunctions. By varying BP thickness, BP/InGaZnO heterojunctions can be operated as forward rectifying diode, Zener diode, and backward rectifying diode, respectively. Room-temperature negative-differential-resistance behavior with large peak-to-valley ratio of 2.1 and high tunneling current density of 160 mA mm^{-2} is obtained in thick-BP/InGaZnO heterojunction. On this basis, sub-thermionic subthreshold swing (SS) of 11 mV dec^{-1} is achieved in InGaZnO TFET. Meanwhile, the InGaZnO JFET based on thin-BP/InGaZnO heterostructure exhibits good transistor performance of on/off ratio exceeding 10^5, high field-effect mobility of 23.5 cm^2 V s^{-1}, negligible hysteresis, and improved *SS* of 83 mV dec^{-1}. The BP/InGaZnO heterojunction is possibly the only device architecture so far to realize the amorphous metal-oxide-semiconductors TFET and JFET, thus providing promising pathways for further thin-film transistor technology.

1. Introduction

Amorphous metal-oxide-semiconductors (AMOSs), such as indium–gallium–zinc-oxide (InGaZnO), have attracted considerable attention due to their advantages in transparency, high carrier mobility, environmental stability, mechanical flexibility, and especially low-temperature process feasibility.[1–5] Inspired by these, metal–insulator–semiconductor field effect transistors (MISFETs) based on AMOSs are widely recognized as a revolutionary display technology for active-matrix displays (AMDs).[2,6,7,8] But as demands grow for AMDs with higher pixel density and lower power consumption, the need for smaller MISFETs with better performance emerges. Till now, most studies focused on suitable material selection, together with carefully optimized processing for transistor miniaturization and circuit thinning.[9–12] However, the aggressively scaled MISFETs face two major challenges. First, the supply voltage cannot shrink with the size of MISFETs, which limits the development of AMOSs in low-voltage, low-power devices.[13,14] This is caused by the degradation in electrostatic control and fundamental thermionic limitation on MISFET turn-on characteristics, that is, subthreshold swing (SS) value of 2.3 K_BT/q; here q, K_B, and T denote the elementary charge, Boltzmann constant, and absolute temperature, respectively. The second, for conventional MISFET, tremendous efforts have been made on ultra-thin dielectric engineering to maintain the gate controllability.[15–17] However, the trap states at uneven dielectric/AMOS interface would interfere with the carrier transport behavior,[18] inducing limited carrier mobility and severe hysteresis. So far, few studies reported that the ubiquitous MISFETs could overcome the serious challenges originating from continuous scaling. Therefore, we need to seek some different transistor mechanism to meet consumer demands.

In this regard, both tunnel field-effect transistor (TFET) and junction field-effect transistor (JFET), in which black phosphorus (BP)/InGaZnO van der Waals (vdW) heterojunctions are employed as fundamental components, are promising

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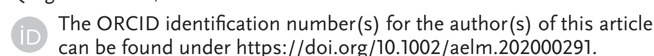
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candidates to replace MISFET for thin-film transistor technology.[18,19] Compared with MISFET relying on thermionic emission (TE) mechanism, TFET employs a fundamentally different conducting mechanism of band-to-band tunneling (BTBT). The carriers tunneling through the heavily doped *p-n* junction enables TFET to exceed the room-temperature limitation of *SS* value of 60 mV dec^{-1}, thus providing the capacity of conquering short channel effect and achieving ultra-low power consumption. In addition, the dielectric is extremely important in determining the electrical properties of AMOS-based MISFET. In comparison, JFET can be switched on and off by modulating the *p-n* junction depletion region with no need for sophisticated dielectric engineering, which can overcome the negative effects of charge trapping at InGaZnO/dielectric interface. In particular, the removal of gate dielectric layer makes JFET resemble MISFET with infinite gate capacitance.[20] For JFET, the *SS* value can be expressed as: $SS = \left[\frac{\partial(\log_{10} I_{ds})}{\partial V_{gs}} \times \frac{\partial \varphi_s}{\partial V_{gs}}\right]^{-1}$, where $\frac{\partial \varphi_s}{\partial V_{gs}} = \frac{C_{gate/channel}}{C_{gate/channel} + C_{source/channel}}$, φ_s denotes channel potential, I_{ds} denotes current between drain and source, and V_{gs} denotes voltage between gate and source.[21] Since the gate-to-channel capacitance ($C_{gate/channel}$) is much larger than the source-to-channel capacitance ($C_{source/channel}$), JFET is expected to outperform MISFET in subthreshold region. However, due to the loose structure of amorphous AMOSs, the methodologies for achieving ultra-sharp doping profile in AMOSs are very challenging. Despite the great interests in AMOSs-based TFETs and JFETs, the two transistors have not been demonstrated yet in experiments.

Recent studies have suggested that 2D atomic crystals are highly promising for TFET and JFET applications,[22–28] owning to their atomic thin body thickness and dangling-bond free surface, which are highly desired to create diverse heterojunctions without the restriction of lattice mismatch. However, little attention has been paid to improving the performance of AMOSs transistors by utilizing the superior properties of 2D materials.

In this paper, we systemically studied the electronic properties of vertically stacked 2D BP/InGaZnO vdW heterojunction diodes. Since the *p*-doping level of BP highly dependent on its body thickness,[23] we can switch the functions of forward rectifying diode, backward rectifying diode, and Zener diodes via simple BP thickness modulation. On this basis, by employing thick BP as electron carrier source and InGaZnO as conducting channel, we demonstrate the InGaZnO TFET with a minimum sub-thermionic *SS* value of 11 mV dec^{-1}, as well as distinct room-temperature negative-differential-resistance (NDR) phenomenon, indicating the presence of BTBT at the vertically stacked thick-BP/InGaZnO interface. Moreover, we also fabricate InGaZnO JFET by constructing thin-BP/InGaZnO vdW *p-n* junction, in which the thin-BP gate enables well-operated n-channel transistor characteristics with large on/off current ratio exceeding 10^5, high field-effect mobility (μ_{FE}) of 23.5 cm^2 V s^{-1}, negligible hysteresis and improved *SS* value of 83 mV dec^{-1}. All of these results evidently demonstrate that the BP/InGaZnO vdW heterojunction based InGaZnO TFET and JFET are highly valuable for future low-power integrated electronics.

2. Results and Discussion

The schematic diagram of InGaZnO transistor based on BP/InGaZnO vdW heterojunction is shown in **Figure 1**a. The TFET operation is based on a thick BP flake attached onto InGaZnO film, where the electrodes 1, 2, and 4 are defined as source, drain, and gate, respectively. On the other hand, the thin-BP/InGaZnO heterojunction is used for JFET architecture, in which the electrodes 2, 3, and 1 are defined as source, drain, and gate, respectively. Here, the vertically stacked BP/InGaZnO heterojunctions are employed for several reasons. First, the presence of vdW gap between BP and InGaZnO can prevent the dopant atoms from diffusing across the heterojunction.

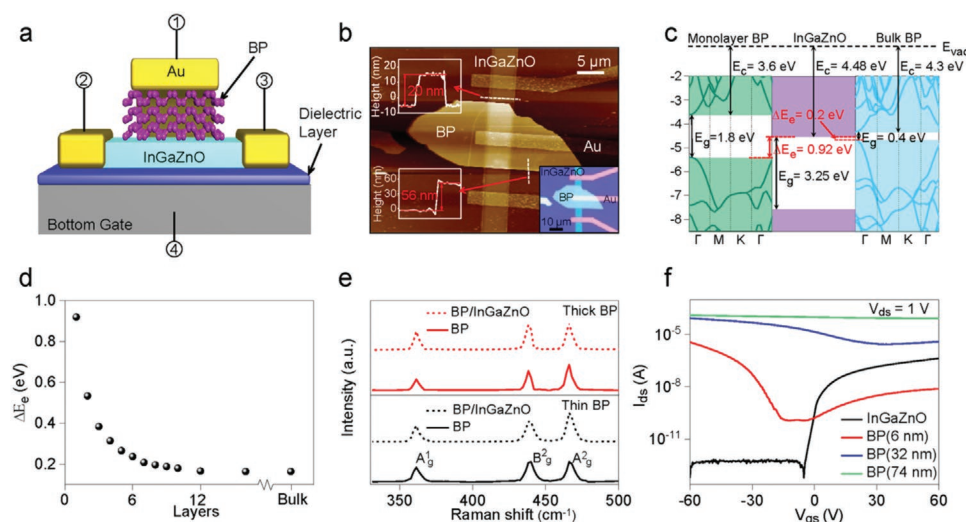

Figure 1. Heterojunction device schematic and material characterization. a) Schematic of InGaZnO transistor based on BP/InGaZnO vdW heterojunction. b) AFM image of the BP/InGaZnO heterojunction. The inset exhibits an optical image of a typically BP/InGaZnO heterojunction. c) Band structures of BP with electron affinities and band gaps obtained from our DFT calculation. The band structure of InGaZnO is taken from ref. [29]. d) The minimum effective bandgap between the VBM of BP and the CBM of InGaZnO. e) Raman characterization of pure BP and the BP/InGaZnO heterojunction. f) Transfer curves of InGaZnO and BP FETs.

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This enables the formation of an ultra-sharp doping profile, and thus a high electric field at the BP/InGaZnO interface. Second, the conventional 3D semiconductor heterojunctions have covalent bonding which could pin the energy band offset at the heterogeneous interface regardless of the doping level and applied bias, unless inserting an insulator layer into the layers. In comparison, in vdW heterojunctions, potential can be dropped across the vdW gap. The band offset of the two materials can be modulated freely by varying the applied drain bias or the electrostatic doping of the gate bias. Third, since BP is attached on top of InGaZnO and a vertical heterojunction is formed, carriers can tunnel through the entire BP/InGaZnO overlap area, which induces a higher BTBT current in InGaZnO TFET than that of lateral heterojunction. For InGaZnO JFET device, this vertical heterojunction is also beneficial for low-voltage operation, since the gate potential can be entirely dropped across the junction so as to avoid the loss in the non-overlap area of lateral heterojunction. Last, because BP is a *p*-doped semiconductor with layer-dependent band gap ranging from 1.8 eV (monolayer) to 0.4 eV (bulk), the energy band offset at BP/InGaZnO junction can be simply modulated by introducing BP layers of different thickness, thus achieving diverse functional BP/InGaZnO heterojunction diodes.

In our experiments, thin InGaZnO film with a width of 5 μm was patterned using e-beam lithography and deposited via magnetron sputtering. The thickness of the InGaZnO film is ≈20 nm, as determined from the atomic force microscopy (AFM) measurement shown in Figure 1b. BP crystal flakes with varying thickness were mechanically exfoliated from bulk BP crystal, and subsequently transferred onto the InGaZnO film. Finally, 50 nm Au electrodes were deposited by thermal evaporation. According to the energy level of BP calculated with density functional theory (see Figure 1c; Figure S1, Supporting Information), the minimum effective bandgap (ΔE_e) between the valence band maximum (VBM) of BP and the conduction band minimum (CBM) of InGaZnO tends to decrease with the increase of the BP flake thickness. The extracted ΔE_e values are 0.92 and 0.2 eV for monolayer-BP/InGaZnO and bulk-BP/InGaZnO heterojunctions, respectively (Figure 1d). In general, the probability of BTBT tunneling transmission ($T(F)$) can be estimated with the equation:[28,30]

$$\mathrm{T(F)} = \exp\left(\frac{-\pi\left(\mathrm{m}^*\right)^{1/2}\Delta \mathrm{E}_{\mathrm{e}}^{3/2}}{2\sqrt{2}\hbar \mathrm{qF}}\right) \tag{1}$$

where m^* denotes carrier effective mass, $\hbar$ denotes the reduced Planck constant, q denotes the elementary charge, and F denotes the applied electric field across the junction. Given small effective bandgap in thick-BP/InGaZnO heterojunction as well as high electric field at the BP/InGaZnO vdW heterojunction interface, BTBT is expected to occur at thick-BP/InGaZnO heterojunction. In comparison, the large effective bandgap in thin-BP/InGaZnO heterojunction simply implies a higher electron thermionic transport barrier, which is highly desirable for JFET operation. Hence, in our experiments, thick BP flake (≈60–80 nm thick) and thin BP flake (≈5–8 nm thick) were employed for InGaZnO TFET and JFET, respectively. Then, the Raman spectra measurements were performed on BP flakes (Figure 1e). The characteristic peaks from pure BP correspond to the A^2_g, B^2_g, and A^1_g modes,[31,32] respectively. The corresponding peak positions at BP/InGaZnO overlap area have neglectable shift, indicating the good interface quality between BP and InGaZnO. Using ≈290 nm thickness SiO_2 as dielectric, transfer curves ($I_{ds} - V_{gs}$) of both BP and InGaZnO FETs are examined (Figure 1f). The InGaZnO FET displays a typical n-type property with an on-off current ratio over 10^6. By contrast, the BP FET fabricated with a ≈6 nm thick flake exhibits an ambipolar transfer characteristic where the hole branch is more pronounced than the electron branch. The on-off current ratio extracted from the hole branch reaches almost 10^4, indicating a non-degenerate doping in thin BP flake. As BP thickness increases, the on-off current ratio is reduced to 1.5 for 74 nm thick BP transistor. This is caused by the degenerate p-type property with a certain BP thickness as demonstrated by the previously reported BP/$SnSe_2$ Esaki diode,[33] that is, the Fermi level of thick BP moves into valence band.

Next, in order to evaluate the possibility of BP/InGaZnO heterojunction for InGaZnO TFET and JFET applications, we study the electrical properties of vertically stacked BP/InGaZnO vdW heterojunction with various BP thickness. **Figure 2**a displays the schematic diagram of the Au/BP/InGaZnO/Au device. The fabrication process and the corresponding optical images are shown in Figure S2, Supporting Information, with the details illustrated in methods section. Here, a completely vertical stack structure, where the current flows directly between the top electrode and the bottom electrode through the heterojunction, is used to eliminate the excess series resistance.[34] Figure 2b,d illustrates the output characteristics of the Au/BP/InGaZnO/Au devices, which exhibit Schottky-like current-voltage ($I_{ds} - V_{ds}$) behavior. In comparison, the Au/BP/Au and Au/InGaZnO/Au vertical devices exhibit almost symmetric $I_{ds} - V_{ds}$ behavior with low Schottky barrier and much higher current density (Figure S3, Supporting Information). Accordingly, we can conclude that the vertical BP/InGaZnO heterojunctions form *p-n* diodes. For the thin BP, the diode exhibits a normal forward rectifying characteristic (Figure 2b). That is, the forward current ($I_{ds(forward)}$) is higher than the reverse current ($I_{ds(reverse)}$), showing a rectification current ratio of 861 at a voltage of ± 2 V. In this case, the thin-BP/InGaZnO heterojunction resembles a forward rectifying diode with a staggered gap band offset. However, as the thickness of BP increases, BP flakes becomes a degenerate p-type semiconductor and the device resembles a *p+-n* diode. There is no essential change in the forward current as shown in Figure 2c. Nevertheless, the reverse current shows a dramatic increase at −1.4 V, which behaves like Zener diode. When the BP thickness continues to increase, the device resembles a *p++-n* diode. The reverse current is larger than the forward current, showing a backward rectifying characteristic (Figure 2d). The corresponding energy band diagrams for these three types of diodes are displayed in Figure 2e. For all three types of diodes, the forward conduction is similar to the conventional *p-n* diode. Under a forward bias, the energy band of BP is pulled down and hence lowers the interface barrier height. As the forward bias increases, electrons in InGaZnO conduction band and holes in BP valence band can drift across the barrier more easily. Therefore, the forward current increases exponentially with V_{ds} according to the equation:[35]

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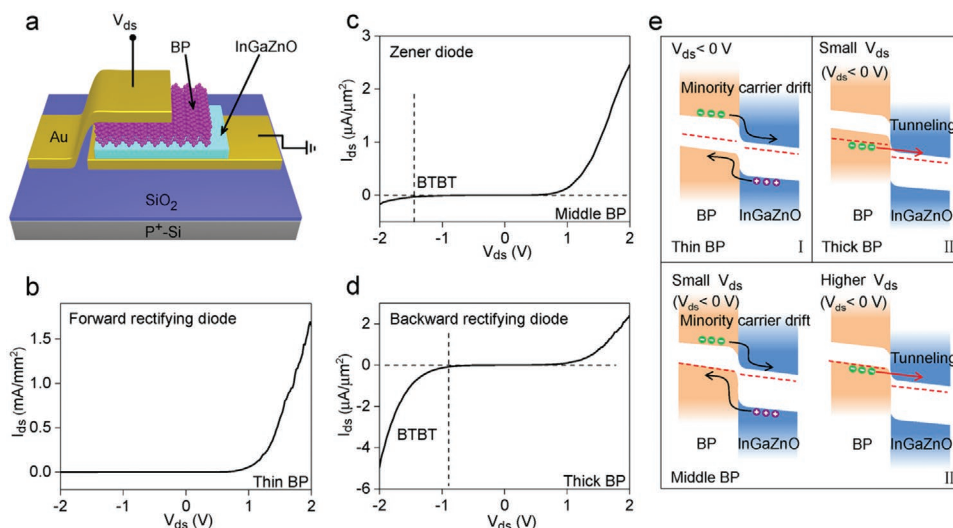

Figure 2. Electrical properties of BP/InGaZnO heterojunction diodes. a) Schematic of BP/InGaZnO heterojunction diode. b–d) Diverse diode properties of BP/InGaZnO heterojunctions composed of BP with different thickness. e) Band diagrams for BP/InGaZnO diodes.

$$I_{\mathrm{ds(forward)}} = I_s \left(e^{V_{ds}/nV_T} - 1 \right) \quad (2)$$

where I_s denotes the reverse saturation current of diode, n denotes the ideality factor, V_{ds} denotes the applied voltage, and V_T denotes the thermal voltage. By contrast, a negative V_{ds} would shift the energy band of BP up and enlarge the interlayer barrier. For the device consisting of thin BP, a type-II band alignment between BP and InGaZnO under a reverse bias could be achieved. In this case, the reverse current is dominated by the minority carrier drift. In view of the strong *p*- and *n*-type characteristics of BP and InGaZnO, respectively, $I_{\mathrm{ds(reverse)}}$ is intrinsically low (Part I of Figure 2e). As the BP thickness increases, the Fermi level of BP is expected to be located near the VBM edge as shown in Part II of Figure 2e. Under a small negative V_{ds}, carrier transport is dominated by the minority carrier drift. However, when a large negative voltage is applied, band alignment between BP and InGaZnO changes from type-II to type-III. At the moment, electrons in BP valence band can tunnel to InGaZnO conduction band due to BTBT, thus resulting in a high reverse tunneling current. For the further thicker BP layers, the energy band alignment of the heterostructure is illustrated in Part III. Due to the higher doping concentration of BP, the electrons tunneling can take place under a small negative V_{ds}. As negative V_{ds} increases, the overlapping of energy level between BP valence band and InGaZnO conduction band is enlarged, which would induce a higher tunneling current. Herein, the thick-BP/InGaZnO heterojunction behaves like a backward rectifying diode.

As described above, forward rectifying *p-n* diode, Zener diode, and backward rectifying diode are achieved based on BP/InGaZnO heterojunctions by varying the BP thickness. Among them, the BTBT in thick-BP/InGaZnO heterojunction is beneficial for the realization of InGaZnO TFETs. Here, we built the InGaZnO TFETs with sub-thermionic *SS* value by employing ≈8 nm Al_2O_3 as high-*k* dielectric (relative permittivity, $\varepsilon_r \approx 9.5$) to provide high gate capacitance. **Figure 3**a shows the vertical heterojunction consisted of a thick BP flake on top of InGaZnO channel, in which the drain electrode is located right on the BP flake while the source electrode is kept away from the overlapped junction region. Prior to the atomic layer deposition (ALD) growth of Al_2O_3 dielectric, a 50 nm-thick Au electrode was deposited on the surface of SiO_2 to serve as the back-gate electrode. According to this device architecture, the multifunctional diodes can be achieved by back gate modulation. Figure 3b exhibits the contour map of output current as a function of V_{gs} and V_{ds}. The rectification ratio is plotted in Figure S4, Supporting Information, correspondingly. We divide the graph into two regions according to the rectification ratio of output current, that is, forward and backward rectifying regions. Notably, a remarkable room-temperature NDR behavior is presented in the forward drain bias direction (Figure 3c), which confirms the BTBT in our thick-BP/InGaZnO heterojunction. The NDR behavior can be explained with the energy band diagram shown in Figure 3d. Because the thick BP is heavily *p*-doped semiconductor, where the Fermi level of BP is located below VBM. At equilibrium state, the CBM of InGaZnO lies slightly below VBM of BP (part I of Figure 3d). Under a small forward drain bias ($0 < V_{ds} < V_{peak}$, part II of Figure 3d), electrons in InGaZnO conduction band would tunnel to the BP valence band, resulting in the BTBT current. Further increasing the V_{ds}, the InGaZnO conduction band tends to align with the BP band gap, and thus the BTBT current decreases. In this case, the TE current starts to dominate the I_{ds} value. As the V_{ds} increases over the V_{valley} (part III of Figure 3d), there is only the TE current over the BP/InGaZnO interface barrier without BTBT. Under a higher forward drain bias ($V_{ds} >> V_{valley}$, part IV of Figure 3d), electrons from the InGaZnO conduction band can tunnel through the triangular BP conduction band via Fowler–Nordheim tunneling, which is confirmed with the $\ln(I_{ds}/V_{ds}^2) - 1/V_{ds}$ plot (Figure S5, Supporting Information).[26,36] In literatures, the reported 2D tunnel devices usually exhibit a NDR trend.[22,23,37] Notably, our vertical heterojunction device shows a clear room-temperature

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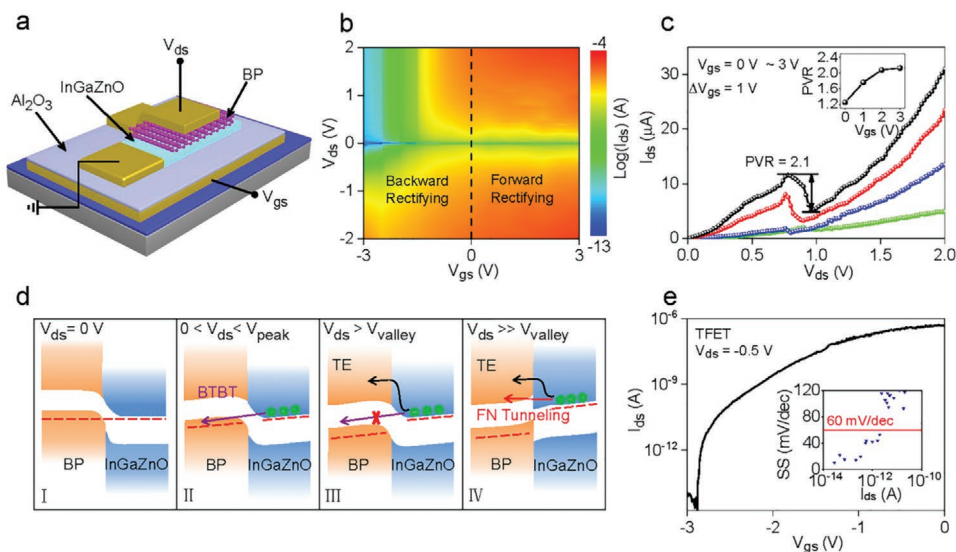

Figure 3. Electrical properties of InGaZnO TFET. a) Schematic of InGaZnO tunnel transistor based on BP/InGaZnO vdW heterojunction. b) The contour map of output current as a function of V_{gs} and V_{ds}. c) Output curve of InGaZnO TFET with NDR behavior under various gate voltages. d) Band diagrams explaining the NDR. e) Transfer characteristics of InGaZnO TFET. The inset shows *SS* values as a function of drain current, in which the red line indicates the fundamental lower limit of *SS* of conventional MISFET.

NDR behavior, indicating an enhanced BTBT effect. The NDR phenomenon observed in tunnel diodes usually requires semiconductors of ultra-high doping, which is widely employed for electronic oscillators. In our device, NDR effect can be further tuned with electrostatic gating. Under a high positive gate voltage of 3 V, the Fermi level in InGaZnO moves further close to its conduction band. The InGaZnO layer thus accumulates more available electron carriers for BTBT, leading a high NDR with peak-to-valley ratio (PVR) of 2.1 (Figure 3c inset). The corresponding peak current density is extracted to be 160 mA mm^{-2}, which is comparable to the conventional Ge or Si homo- or heterojunctions (Figure S6, Supporting Information).[38–42] Figure 3e shows the transfer characteristics of the device. It is observed that the device is switched on rapidly within a very small gate bias range, which overcomes the fundamental limitations on SS in MISFETs. The SS value of the device is plotted in Figure 3e inset. Here, the SS values below 60 mV dec^{-1} are achieved over about three decades of current. The lowest *SS* achieved for the device is ≈11 mV dec^{-1}, which demonstrates that the InGaZnO TFETs can potentially address the energy-efficiency requirement.

Besides TFET, JFET is also a promising alternative to MISFET for low voltage operation and low power consumption. From the forward rectification diode characteristic of Figure 2b, we noticed that the JFET can be realized with slight adjustment of the vertical diode structure. In our experiments, in order to clearly demonstrate the distinguish between MISFET and MESFET, we fabricated thin-BP gate InGaZnO JFET and InGaZnO MISFET with ultra-thin 5.5 nm ALD Al_2O_3 top gate dielectric, while these two devices were prepared on the same substrate, as shown in the schematic diagram of **Figure 4**a. The electrical characteristic of the thin-BP/InGaZnO vdW heterojunction is shown in Figure 4b, which exhibits excellent forward rectification diode behavior with on/off current ratio of ≈10^3 and ideality factor of ≈2.2. The transfer characteristics of the two transistors are shown in Figure 4c,d, where MISFET exhibits ≈three times higher output current than JFET measured at V_{ds} = 1 V. However, the output current of JFET can be enhanced via back-gate coupling effect. As shown in Figure S7, Supporting Information, with a positive back-gate bias of 60 V, the output current is increased by ≈ten times while the threshold voltage (V_{th}) shifts to a more negative value. This is understandable since InGaZnO has higher carrier concentration and exhibits higher conductivity via the back-gate electrical doping, and thus a more negative top-gate bias is required to deplete InGaZnO channel. On the other hand, due to the serious trap-induced interface scattering,[18] the field-effect mobility of MISFET is limited to ≈4.8 cm^2 V s^{-1}, together with large *SS* value of 91 and 103 mV dec^{-1}, too much negative V_{th} of −0.85 and −1.75 V, and large hysteresis of ≈0.95 V, while JFET exhibits high mobility of ≈23.5 cm^2 V s^{-1}, improved *SS* value of 83 mV dec^{-1}, slightly negative V_{th} of −0.73 V, and neglectable hysteresis of ≈0.06 V. The hysteresis in InGaZnO MISFET can be attributed to the trapping of carriers from the gate bias-induced conduction channel into less mobile localized states.[24,43] We have summarized the performance parameter values for JFET and MISFET into Table S1, Supporting Information. The field-effect mobility (μ_{FE}) for MISFET can be calculated from the device transfer curves, based on the equation below:

$$\mu FE = g_m \left(\frac{L_2}{C_{ox}}\right)\left(\frac{1}{V_{ds}}\right) \quad (3)$$

where g_m denotes the low-bias transconductance, C_{ox} denotes the gate capacitance, and *L* denotes the channel length. The μ_{FE} value for JFET are estimated by the expression:[24]

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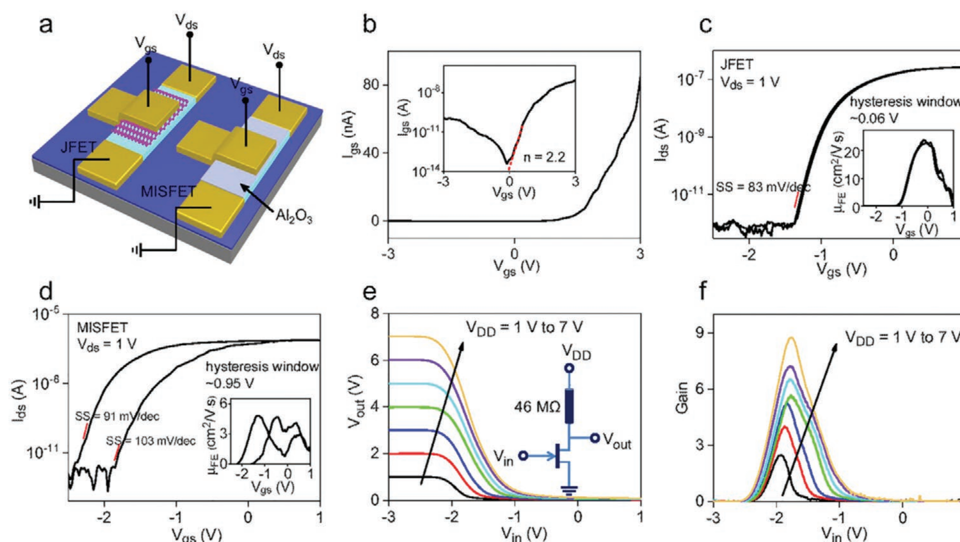

Figure 4. Device schematic and electrical characterization of InGaZnO JFET and MISFET. a) Schematic of InGaZnO JFET and MISFET. b) $I_{gs} - V_{gs}$ curve of BP/InGaZnO heterojunction diode. c) Transfer curve of InGaZnO JFET. The inset shows the corresponding μ_{FE} value. d) Transfer curve of InGaZnO MISFET with 5.5 nm Al_2O_3 dielectric layer. The inset shows the corresponding μ_{FE} value. e) Voltage transfer characteristics of the inverter. The inset shows the schematic drawing of the equivalent electronic circuit. f) The extracted voltage gain of the inverter. At V_{DD} = 7 V, the peak voltage gain is about 8.8.

$$\mu_{FE} = \frac{Lg_m}{qN_d tw} \tag{4}$$

where N_d denotes the electron carrier density of InGaZnO, W and t denote the channel width and thickness, respectively. The N_d value can be estimated using the Padovani–Stratton parameter method (Figure S8, Supporting Information). The corresponding output curves are displayed in Figure S9, Supporting Information. The JFET exhibits well saturation behavior arising from the easy channel depletion at drain side, while MISFET exhibits almost completely linear. In addition, a resistive-load inverter composed of InGaZnO JFET and external resistor was fabricated to extend the usage of our JFET toward further practical application. The voltage gain of an inverter greater than 1 is important for the application of cascade logic circuit because it makes the circuit regenerative and robust to errors. The gain is usually defined as gain = $-dV_{out}/dV_{in}$, where V_{out} and V_{in} are output and input voltages, respectively. The JFET inverter shows excellent voltage transfer characteristics under a wide range of supply voltage (V_{DD}) (Figure 4e). Figure 4f exhibits the extracted voltage gain of the inverter, a maximum value of ≈8.8 is achieved at V_{DD} = 7 V. The excellent JFET operation can mainly be attributed to the BP/InGaZnO vdW interface, protecting InGaZnO channel from any mutual influence.[25]

3. Conclusion

In conclusion, we demonstrate InGaZnO TFET and JFET based on vertically stacked BP/InGaZnO vdW heterojunctions. A room-temperature NDR behavior in thick-BP/InGaZnO heterostructure system is obviously observed. By employing thick BP as electron carrier source and InGaZnO as conducting channel, we demonstrate InGaZnO TFET with a sub-thermionic subthreshold swing of ≈11 mV dec^{-1}. By contrast, the thin-BP/InGaZnO heterostructure exhibits typical forward rectifying characteristic. Using thin BP as gate, the InGaZnO JFET exhibits well transistor operation with on/off ratio exceeding 10^5. In JFET, the carrier transport behavior may hardly be affected by charge traps at uneven dielectric/InGaZnO interface. Accordingly, the device exhibits high field-effect mobility of 23.5 cm^2 V^{-1} s^{-1}, together with negligible hysteresis and improved SS value of 83 mV dec^{-1}. Our proposed BP/InGaZnO heterojunction based InGaZnO TFET and JFET therefore suggest promising possibility for future low-power integrated electronics.

4. Experimental Section

Atomic Layer Deposition Growth of Al_2O_3: ALD growth of Al_2O_3 was carried out employing trimethylaluminum (TMA) and H_2O precursors at 100 °C. The carrier gas was highly purified Ar. During the depositing process, the temperature of the H_2O source and TMA source were 25 °C. The purge of TMA and H_2O precursors were applied with highly purified Ar for 5 s. The growth rate of Al_2O_3 is approximately 1 Å per cycle.

Device Fabrication and Measurements: For the preparation of vertically stacked BP/InGaZnO vdW heterostructure diode, a 50 nm-thick Au bottom electrode was first deposited onto a marked p^+-Si/SiO_2 substrate (SiO_2 thickness ≈ 290 nm) by metal evaporation. After patterning by electron beam lithography, a 20 nm-thick InGaZnO film was deposited onto the Au electrodes by magnetron sputtering with a single target (In_2O_3:Ga_2O_3:ZnO = 1:1:1 atom%). During the sputtering deposition, the DC power was 20 W, the Ar flow rate was 12 sccm, and the gas pressure was 0.7 Pa, respectively. Subsequently, BP flakes were obtained using mechanically exfoliated method and then transferred onto the InGaZnO film. At the end, a 50 nm-thick Au top electrode was formed by electron beam lithography and metal evaporation process.

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Similarly, the fabrication of the InGaZnO TFET based on vertically stacked thick-BP/InGaZnO heterojunction was initiated by defining Au bottom electrode onto a marked p^+-Si/SiO_2 substrate. Then, a ≈8 nm-thick Al_2O_3 layer was deposited by ALD as bottom gate insulator. After that, the InGaZnO film was deposited onto the prepared Al_2O_3 layer. The exfoliated thick BP was then transferred onto the InGaZnO film. Finally, Au electrodes were deposited onto BP flake and InGaZnO film by metal evaporation and the lift-off process. The channel length and width of the TFET is 6 and 5 µm, respectively.

For the fabrication of InGaZnO JFET and MISFET, the InGaZnO film was first deposited onto a marked SiO_2/P^+-Si substrates under the same sputtering conditions. Then, source/drain electrodes (50 nm thick Au) were deposited onto the InGaZnO film. The channel length and width of the JFET and MISFET were 25 and 5 µm, respectively. After that, thin BP was transferred onto InGaZnO as JFET gate electrode and a 5.5 nm-thick Al_2O_3 layer was deposited by ALD as MISFET top gate insulator. At the end, the Au top gate electrodes were deposited onto BP and Al_2O_3 layer, respectively.

Electrical measurements were carried out with Lake Shore TTPX Probe Station and Agilent B1500A semiconductor parameter analyzer under vacuum condition (≈1.0×10^{-3} Pa). The AFM analysis was performed using Bruker Multimode 8. Raman spectra are recorded with a micro-Raman system (Horiba LABHR) excited by 532 nm laser.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

black phosphorus, indium–gallium–zinc-oxide, junction field-effect transistors, thin-film transistors, tunnel field-effect transistors

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